Challenges and Opportunities in Electronic Packaging

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Agenda

Introduction

Microelectronics in Our Daily Lives

What is Integrated Circuit Packaging?

Technology Challenges and Trends …

Opportunities in IC Packaging & Board Technology Development
Our Mission: Making Package, Test, and Board Leadership Technology Affordable for all of Intel’s Products
Where does IC Packaging fit into the scheme of things ...

Product Design ...

Silicon/Sort ...

Package/Test ...

Circuit Board/Test ...

System/Test ...

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Micro-electronics have become ubiquitous
Today

The environment is much more complex ...

- Large number of diverse applications ...
- Segmentation in Product Design, Performance Demands, How components/devices are used, Cost Sensitivities

- Package/Board & Test Technology must enable:
  - Wide range of Form Factors
  - Interconnect Scaling
  - High Speed Signaling
  - Power Delivery & Thermal Solutions
  - Complex Silicon/Package Integration
  - Materials technologies to meet demands on performance and end-user reliability
  - HVM @ affordable cost

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Increase in Socket Pincount
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**What is Integrated Circuit Packaging?**

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Development
Why is Electronic Packaging Important?

The Early Role of Packaging

Dual In-Line Package

1st Design Win
Busicom Calculator

Silicon to Package

Package to System

The Package was just the Middleman... Providing space transformation and environmental protection
Today, the role is much more complex ...

1. **I/O connection**
2. **Power Delivery**
3. **Power Removal**
4. **Customer Ease-of-Use/Inventory Control**
5. **Protect the chip**

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Package Examples

Intel Core 2 Duo

Pentium II

Intel Core 2 Quad

Atom Z5xxP

Pentium processor with MMX technology
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Challenge – Thin, Thin, Thin to achieve More Performance/millimeter$^3$

Convergence Increases level of Integration... Requires Thin Wafers, Die, and Substrates to fit consumer electronics needs
Package Scaling

FLI Technology Trends

Signal Escape per Layer

2 Track
1 Track

Signal Density

Package Design Moved to Single Track Routing with FCxGA10 Due to Signal Integrity Concerns

Circuit Density & Power Delivery Requirements Required Increasing Density Beyond FCxGA8

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Packaging Key Drivers

Deliver the Lowest Total Product Cost (Die + Package) while satisfying functional requirements

Stay in the ‘sweet spot’ of supplier and customer capabilities

Key Focus Areas

Meet/Exceed functional performance targets
Align the ‘right’ technology to the product requirement
Achieve Best in Class Die Size

Optimize bump/pad pitch and patterns for Density and alignment to substrate capabilities

Minimize Package Size/Cost

Optimize solder ball placement for motherboard routing
Recognize where advanced motherboard technology can deliver better end user value

Die Size vs. Package Cost Trade-Offs for Lowest Total Cost
FLI Global IO Density

FLI Global IO Density is a useful gauge of package capability.

Calculated by Dividing Signal Count by Die Perimeter

Random Example:

Signal Count = 418
Die Perimeter = 39.4 mm

FLI Global IO Density = 418/39.4 = 10.61 IO per mm
FLI Local IO Density

FLI Local IO Density is distinct from FLI Global IO density

FLI Local IO density calculated by dividing signal count for a given IO unit cell by the width of the unit cell

FLI Local IO density will always be greater than FLI Global IO density

Corner effects

Not all interfaces are created equal – some interfaces have greater FLI Local IO density than others

FLI Local IO Density directly drives FLI interconnect technology

Bump Pitch, Substrate Line/Space, Substrate Layer count, etc
FLI Local IO Density Example

In this example FLI Local IOD = 5 signals/Unit Cell Width
FLI Local vs. Global IO Density Comparisons

- Local FLI IO Density
- Global FLI IO Density
- Efficiency

IO Density - IO per mm

IO Density Efficiency

X A B C D

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Why use die perimeter for IO Density Calculations?
Why use die perimeter for IO Density Calculations?
A more realistic case

FC-BGA Substrate Routing Example (5 Signals Deep per Unit Cell)

- Inner Substrate Layer Signal Routes
- Top Substrate Layer Signal Routes
- Die Edge
- Unit Cell Boundary
- Bump Pad
- Die Core
- Bump Pitch
- Package Layer Color Code from Previous Slide

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Factors that influence FLI Global IO density trends

- **Silicon Process Scaling**
  ~ 30% per Generation (linear)

- **Transistor Count**
  Trend varies by product

- **Signal Count**
  Function of bandwidth & Interface technology

**How rapidly does FLI IO density need to grow?**
Graphics complexity driving transistor count growth faster than Moore’s Law
Die size has grown even as silicon geometries have reduced.
Enabling Integration - Mechanical Integrity

From Nanometer to Millimeter...

…Understanding and Managing Mechanical Integrity Over Changes in Scale is Critical
Analytical Capabilities & Challenges

- **Continue to Evolve Current Analytical Tools (e.g., Improved Predictability, Increased Resolution)**
- **Focus Research on Non-destructive Methods (e.g., Thermal Imaging)**
Material handling & transport challenges increasing as wafer/dice & substrate get thinner

Precision control of die attach force, position, and underfill process to reduce package form factors

Focus areas:
- Cap Placement
- Epoxy Tongue
- Package Marking
- Test Socket
Innovation in Materials Technology Examples ...
Testing Challenges

The semiconductor devices are subjected to a variety of electrical tests to determine if they function properly and meet desired performance requirements.

So the question for test technologists is: How can test cost per unit be kept flat (or driven lower) while the technology being tested is becoming exponentially more complex?
Future Cost Challenges

- **Product Price Erosion Is a Reality of Life**
- **Innovative Package Architectures are Required to Meet Performance Challenges While Reducing Cost**

Unconstrained Product Cost (Driven by Complexity)

Margins

Average Sales Price

Time

Margins

Average Sales Price

Time

Product Price Erosion Is a Reality of Life

Innovative Package Architectures are Required to Meet Performance Challenges While Reducing Cost
Package Thermal Capability
Reductions in Thermal Resistance Enable Products

Phase change materials, New solder and polymeric interface materials, Novel coatings, Control of filler particle properties (size, surface, volume fraction, etc); Improved IHS attach process; Etc.

Improvements made to thermal capability of packages enable products to meet increased thermal demands due to circuit scaling.
Thermo-mechanical Stress Failures

- Die Cracking
- Die Buffer Coat Cracking
- Si Interlayer Dielectric Cracking
- Interconnect Solder Fatigue
- Substrate Cracking
- UF Cracking
Stress Compensation Layer Technology

- Innovated new technologies to place layer of stress compensation layer material between BGA solder balls.
- Resulted in significant improvement in shock performance.
Smart Materials

- Materials that respond to external stimuli.
- Typically have a specific response with a specific trigger.
- Examples:
  - Shape memory materials
  - Self-healing materials
  - Adhesion/wetting on demand

Source: www.tinialloy.com/livewire.html
• **Self Healing Polymers** - Research technology with potential for significant increase in toughness.
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Other Examples of Technology Development Challenges

• Materials development & characterization for performance and cost requirements
  - Package substrates; Thermal interface materials; Novel solder materials; etc
  - Improved interface characterization and Time and temperature dependent material properties

• Electrical Analysis and Design
  - High speed signaling & Power Delivery
  - Time and Frequency domain analysis and measurements for validation and characterization

• Mechanical response and integrity of complex material systems
  - Analysis & Validation of heterogeneous material systems & multi-scale domains subject to static and dynamic loads

• Integrated systems design and analysis
Opportunities - Universities

• **Continue to Produce High Caliber Students**
  • Emphasize Basics of Education to Ensure Adaptability to a Changing Environment

• **Focus Research**
  • Generate Solution Strategies to New Industry Challenges
  • New Modeling, Analytical and Characterization Tools and Techniques... Leave Proliferation and Usage to the Industry

• **Use Industry Partners to Validate Research Strategies and Accelerate Technology Transfer**
Questions?
Package Scaling
FLI Bump Pitch Trend

IO Circuit Area Scaling

IO Bump Pitch Scaling

87% Linear Scaling Supports Historical ~75% IO Circuit Area Scaling
Thermal Solutions
Impact of Non-Uniform Power

Different parts of the die require varying amounts of power → Non-uniform power distribution

R\textsubscript{jc} = package thermal impedance under uniform heating (°C cm\textsuperscript{2}/W)
Ψ\textsubscript{jc} = package thermal resistance under non-uniform heating (°C/W)
DF accounts for both die size and non-uniform heating

Higher equivalent TDP that needs to be cooled