







Welcome to the Intel Asia Academic Forum 2007

We are pleased to welcome you to the Intel Asia Academic Forum 2007. Organized under the Intel® Higher Education Program, this forum gathers key Intel technical experts and top professors from select Asian universities in China, India, Japan, Malaysia, Philippines, Taiwan and Vietnam to exchange ideas on current technology trends and challenges. Our theme for this year is "Accelerating Innovation & Research on Emerging Technologies".

The objectives of the forum are to:

- Showcase Intel's technology roadmap, business and research directions.
- Increase participants' understanding on Intel's R&D programs and activities.
- Showcase exemplary work of faculty in curriculum development and research.
- Discuss the challenges faced by industry, government and academia.
- Foster an environment for interaction and collaboration between academia and Intel technologists.

The Intel Asia Academic Forum 2007 will have keynotes and 4 tracks focused on:

- Technology & Manufacturing
- Systems and Architecture,
- Software for Multi Core and
- Emerging Technologies.

Besides the technology session, the forum will also host a session for government, academia and industry titled "Transcend to Emerging Technologies" on 26th October 2007. This session will deliberate on challenges faced in proliferation and adoption of new technologies.

A vital feature of the forum's agenda is a series of sessions which combine networking topics and poster display. These are two poster sessions that feature research and curriculum development undertaken by participating university professors. We encourage participants to go around and engage in these discussions with Intel experts and fellow academic researchers.

The Asia Academic Forum 2007 has received overwhelming participation from Intel Fellows, Intel VP's, Director's, Principal Engineers, and technologists from relevant Corporate and Asia business groups.

We look forward to meeting you in what promises to be a most fruitful, stimulating and, at the same time, enjoyable event.

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Brenda Musili President, Intel Foundation Director, Worldwide Education

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Intel Asia Academic Forum 2007 October 24 - 26,2007, New Delhi

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ACKNOWLEDGEMENTS

It would not be possible to run an event of this magnitude and complexity without the support of many individuals and groups. We would like to acknowledge a few people who have made this event possible.

Firstly, we would like to acknowledge the contribution made by our distinguished speakers. It wouldn't have been possible to have an agenda with keynotes and parallel tracks without the support received from Intel Fellow's, Intel VP's, Intel's Principal engineers, Intel Researchers and other senior Intel leaders. We would like to thank all of them for taking time from their busy schedule, doing long travels from across sites and supporting AAF 2007.

A special thanks to the Intel Technologists who are part of the Technical Chair for compiling and setting the context of the Asia Academic Forum. The Technical Chairs has been part of the forum from the planning through the execution of the forum.

We would also like to additionally recognize our external stakeholders from the academia, government, industry and apex bodies for their participation in AAF 2007. Thanks to the delegates from the academia who took time to attend the forum and present their research & curriculum work at the poster sessions at AAF 2007.

A big thanks to the Intel Global education team, Asia education team, Asia Higher Ed managers, Intel India staff, Corporate and Asia business groups and the for all the support & encouragement provided in organizing AAF 2007.

Thanks to everyone!

Intel Asia Higher Ed Team

(intel[®]) Education



Intel Asia Academic Forum 2007 October 24 - 26,2007, New Delhi

AGENDA

Date: 24th October 2007

6:30am - 7:30am 7:30am - 8:15am	Breakfast Travel to India Habitat Cente	er (IHC)	
Time	Session Title	Speaker	Designation
Keynotes			
8:30am - 8:45am	Welcome & Inauguration	Praveen Vishakantaiah	President Intel India
		Sunit Tyagi	Director of Technology, Intel India
8:45am - 9:35am	Beyond the blackboard: Technology and Teaching in the 21st Century	Rob Crooke	Vice President, Sales & Marketing, General Manager, Business Client Group
9:35am - 10:25am	Extending Moore's Law with Innovations in Nano-scale CMOS Technologies	Kevin Zhang	Intel Fellow and Director of Advanced Memory Circuit and Technology Integration at Intel Technology & Manufacturing Group
10:25am - 10:45am	n Tea Break		
10:45am - 11:35am	Energy-Efficient Terascale Computing in Nanoscale Technology: Emerging Challenges and Opportunities	Vivek De	Intel Fellow and Director of Circuit Technology Research in Intel's Circuits Research Lab (CRL)
11:35am - 12:25pm	A Review of Emerging Memory Technologies	Valluri Rao	Intel Fellow, Technology Manufacturing Group, Director, Analytical and Microsystems Technologies
12:25pm - 1:15pm	SoC architectures in TeraScale World: Challenges and Opportunities	Raj Yavatkar	Intel Fellow and Director of the Platform Validation Architecture in the Digital Enterprise Group

Break in to Parallel T	racks		
Track 1 : System	s & Architecture		
2:15pm - 3:00pm	Intel® Trusted Execution Technology (TXT)	Anand Rajan	Re: Sta
3:00pm - 3:45pm	Systems Packaging: Multi-Disciplinary Challenges	Arun Chandrasekhar	Sta Dig
3:45pm - 4:00pm	Tea Break		
4:00pm - 4:45pm	UMD usage models, technology requirement and research challenges	Krishna Paul	Sof Ult
4:45pm - 5:30pm	Panel discussion (Anand Raja James Reinders + 3 faculties)	in, Kumar Rangana)	thar
Track 2 : Technol	ogy & Manufacturing		
2:15pm - 3:00pm	Systematic Innovation in Manufacturing - challenges/ strategies	TS Yeoh	Prii Ass Ma Tes
3:00pm - 3:45pm	Highly Productive Assembly and Test Manufacturing in the Nano-Technology Era	Jeff Pettinato	Ser Eng and Gro Au Pat Ass Teo Dev
3:45pm - 4:00pm	Tea Break		
4:00pm - 4:45pm	Challenges & Opportunities in Electronic Packaging	G Sreenivas	Gei Teo Ma Ino
4:45pm - 5:30pm	Panel discussion (Kevin Zhan Jeff Pettinato)	g, Valluri Rao, G Sr	een

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aff Architect, gital Enterprise Group

ftware Architect, tra-mobile group

n, Raj Yavatkar,

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nior Principal gineer, Technology d Manufacturing

roup utomation Strategy & athfinding Manager, ssembly Test echnology evelopment

neral Manager, chnology anufacturing Group dia

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5:30pm - 7:30pm	Poster Session
7:30pm - 9:30pm	Dinner at India Habitat Centre
9:30pm - 10:30pm	Tour: Delhi by the Night
10:30pm - 11:00pm	Travel back to Hotel

Date: 25th October 2007

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6:30am - 7:30am	Breakfast		
7:30am - 8:15am	Travel to India Habitat Cente	r (IHC)	
Time	Session Title	Speaker	Designation
Keynotes			
8:30am - 8:45am	Welcome Day 2 & Key Announcements		
8:45am - 9:35am	Mobility-Redefined	Mary Smiley	Director, Emerging Platforms Lab (EPL), Corporate Technology Group
9:35am - 10:25am	Human Centered Innovation	Herman D'hooge	Innovation Strategist Intel Research
10:25am - 10:45am	Tea Break		
10:45am - 11:35am	Software for multi-core processors.	Vittal Kini	Director of Research, Intel India
11:35am - 12:25pm	CMPC: Integrating Technology for Local Markets	Tom Rampone	Vice president of Sales and Marketing Group and General Manager of the Channel Platforms Group
12:25pm - 1:15pm	Exploratory Research: Essential Computing – Computing for the Essence of our Lives	Andrew Chien	Vice President of Intel Research
1:15am - 2:15pm	Lunch		

Break in to Parallel Tracks			
Track 3 : Softwa	re for Multicore		
2:15pm - 3:00pm	Exploiting Parallelism with Multi-core Technologies	James Reinders	Chi Dire
3:00pm - 3:45pm	Compiler challenges for future computing platforms	Milind Girkar	Prir
3:45pm - 4:00pm	Tea Break		
4:00pm - 4:45pm	Parallelized XML Processing	Young Wang	Mai eng
4:45pm - 5:30pm	Concurrency Control in Managed Runtimes	Suresh Srinivas	Prir
Track 4 : Emergir	ng Technologies		
Track 4 : Emergin 2:15pm - 3:00pm	ng Technologies Sensing and making sense: the new challenges of healthcare information systems	JM Van Thong	Ser Eng Teo Can
Track 4 : Emergin 2:15pm - 3:00pm 3:00pm - 3:45pm	ng Technologies Sensing and making sense: the new challenges of healthcare information systems Rural Wireless Connectivity: Technologies and Challenges	JM Van Thong Ajay Bakre	Ser Eng Tec Can
Track 4 : Emergin 2:15pm - 3:00pm 3:00pm - 3:45pm 3:45pm - 4:00pm	ng Technologies Sensing and making sense: the new challenges of healthcare information systems Rural Wireless Connectivity: Technologies and Challenges Tea Break	JM Van Thong Ajay Bakre	Ser Eng Tec Can
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Track 4 : Emergin 2:15pm - 3:00pm 3:00pm - 3:45pm 3:45pm - 4:00pm 4:00pm - 4:45pm 4:45pm - 5:30pm	ng Technologies Sensing and making sense: the new challenges of healthcare information systems Rural Wireless Connectivity: Technologies and Challenges Tea Break VLSI Process Technology Panel Discussion	JM Van Thong Ajay Bakre Sunit Tyagi	Ser Eng Tec Can Inte

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Date: 26th October 2007 (Session on Emerging Markets)

Time	Session Title	Speaker	Designation	
Keynotes				
9:00am - 9:45am	Welcome	Rahul Bedi	Director Corporate Affairs, South Asia	
	Intel's Technology Direction in India	Praveen Vishakantaiah	President Intel India	GS
9:45am - 10:00am	Semiconductor Industry in India	Poornima Shenoy	President, India Semiconductor Associatio	ETIN
10:00am - 10:30am	Role of Government in taking Broadband to the masses	Shantanu Consul	Administrator (USF), Department of Telecommunications, Govt of India	N ONE ME
10:30am - 11:00am	Challenges for Kiosk model	R. Chandrashekar	Administrator (USF), Department of Telecommunications, Govt of India	ONE ON
11:00am - 11:30am	Tea Break			N S
11:30am- 12:00pm	Trends in Research & Engineering Education in India	V.Rao.Aiyagari	Adviser & Head (SERC), Department of Science & Technology, Govt of India	SESSIO
12:00am- 12:30pm	Intel's research collaboration model with Govt in Ireland	Frank Turpin	Corporate Affairs, Intel Ireland	TERS
12:30pm- 1:15pm	Industry & Academia Collaboration: India Multi core Case Study	Sanjeev Aggarwal	Professor, Department of Computer Science, IIT Kanpur	POS ⁻
		Manav Subodh	Manager, University Programs, Intel India	
1:15am - 2:15am	Lunch			

Time	Session Title	Speaker	Designation	
Keynotes				
2:15pm- 3:30pm Panel Discussion on Challenges & Opportunities in Emerging Markets	Panel Discussion on Challenges & Opportunities	Sivakumar Ramamurthy	Managing Director, Intel South Asia	
	Tom Rampoone	Vice President of Sales and Marketing Group and general manager of the Channel Platforms Group		
		Kentaro Toyama	Microsoft Research	
		Apala Chavan	VP Asia, HFI	_
		Ganesh Prabhu	IIM Bangalore	All
3:30pm - 4:00pm	Tea Break			C
4:00pm- 5:30pm Panel Resea	Dpm Panel Discussion on Research Challenges and	Vittal Kini	Director of Research, Intel India	CITV
	needs from India Innovation Policy	Andrew Chien	Vice President Intel Research	
		D.K. Subramanian	President FAER	
		Sanjay Dhande	Director, IIT Kanpur	
		V.Rao.Aiyagari	Adviser & Head (SERC), Department of Science & Technology, Govt of India	
			IBM Research	

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AAF 2007 AFTER HOURS

One of the objectives of this forum is to facilitate communication, foster exchange of ideas and initiate collaboration. The Intel Asia Academic Forum (AAF) 2007 will provide opportunity for academic delegates to showcase relevant research and curriculum developments.

You are invited to a showcase of break through accomplishments and best known methods by various countries through poster sessions. You can visit www.intel.com/education/aaf07 to view 54 selected posters submitted by faculties from all across Asia . The posters presented on the website and a few more will also be displayed on the evening of 24th October 2007 at AAF 2007. Participants can also request for a one on one meeting with the faculties based on their individual interests. These meetings will be held on 26th October, 9am-1:15pm, at AAF 2007.

Get ready to participate in an enthralling evening and gala dinner on 25th Oct 2007. In an endeavor to promote social ventures that have a wide social impact; Intel Higher Education is inviting selected entrepreneurs from academia to showcase applications that have a great potential to solve grassroot problems & take IT to the masses. You can get an opportunity to meet them at the gala dinner and later get to see their products and demos on 26th Oct 2007.

On 26th Oct at AAF 2007 we would like to invite you to an industry, academia and government session titled Transcend to Emerging Technologies. You can get an opportunity to hear some of India 's senior government officials, thought leaders, Intel and industry experts on some of the best practices and challenges relevant for emerging markets. In parallel and for participants who wish to utilize their time for networking; we will continue with the poster presentations and structure meetings

AAF 2007 AFTER HOURS

We look forward to hosting you at India for AAF 2007. As you step into the new India which is blazing an economic growth trail, you will also see a glimpse of the old traditional India . Behind the sheath of centuries of transformation, is hidden the wonders of India 's rich scientific heritage. At Intel Asia Academic Forum 2007, we will strive to take this resonance to another level.

Welcome to the Intel Asia Academic Forum 2007!

Manav Subodh Program Manager- AAF 2007 India Higher Ed Manager

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SPEAKER PHOTO, **BIO'S AND ABSTRACTS**





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Rob Crooke Vice President, General Manager, Business Client Group

Robert Crooke is vice president and general manager of the Business Client Group (BCG). He is responsible for directing Intel's vision for delivering innovative business client solutions and is responsible for the definition, development, and marketing of Intel's

desktop platform solutions.

Previously, Crooke served as vice president and general manager of the Desktop Product Group, leading the marketing and planning of Intel's desktop products and initiatives. This includes the processors and chipset product roadmaps as well as digital home and digital office initiatives. From 2000 to 2004 Crooke was general manager of the Platform Architecture and Solutions Division. In this role he was responsible for the company's development of motherboard products in addition to desktop microprocessor and chipset enabling technology, which includes reference platforms, as well as electrical and thermal mechanical solutions. Crooke has served as director of marketing for the Basic Microprocessor Division and Performance Microprocessor Division. He joined Intel in 1989 in the sales force as a field applications engineer and spent nine years in the field in various roles.

Crooke is a frequent speaker at industry events, including the Intel Developer Forum, Communication Board of Directors, Game Developers Conference and the Consumer Electronics Show. Prior to joining Intel, he held design engineering positions at Alliant Computer Systems and Custom Silicon Inc. He received his bachelor's degree in computer systems engineering from the University of Massachusetts in 1985.

Presentation Abstract

Presentation Title:	Beyond the blackboard: Technolog
	in the 21st Century
Presenter Name:	Rob Crooke
Job Title:	Vice President, General Manager,
	Business Client Group

Abstract:

Technology is dramatically changing the knowledge being produced in the world today. These technological changes, which will be as fundamental as the introduction of blackboards into the classroom two centuries ago, will test the academic structures around the world. Intel has established a leadership role with the World Ahead Program to offer a scalable and cost effective solution for developing nation academic structures. Mr. Crooke will discuss the importance of accelerating access to the World Ahead Program technologies and how these new Intel innovations will focus on building 21st century skills for today's children, today's educators and tomorrow's working citizens.

y and Teaching





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Kevin Zhang

Intel Fellow and Director of Advanced Memory Circuit and Technology Integration at Intel Technology & Manufacturing Group

Kevin Zhang is an Intel Fellow and Director of Advanced Memory Circuit and Technology Integration at Intel Technology & Manufacturing Group. He is responsible for Intel's embedded memory technology development for future products. Zhang has led the

design and validation of technology lead vehicles for both future process and product development from 90nm to 45nm generations at Intel. Zhang received his BS degree from Tsinghua University in 1987 and his PhD degree from Duke University in 1994, both in Electrical Engineering.

Presentation Abstract

Presentation Title	: Extending Moore's Law with Inno
	scale CMOS Technologies
Presenter Name	: Kevin Zhang
Job Title	: Intel Fellow and Director of Advar
	Circuit and Technology Integration
	Technology & Manufacturing Grou

Abstract:

Moore's law has been the guiding principal for semiconductor industry over last 40 years. The relentless technology scaling has reduced the feature size of transistor well blow 50nm regime in today's CMOS technology and the scaling has led to an unprecedented level of integration in VLSI system design in achieving ever higher performance and lower power consumption. As the physical dimensions of transistors are scaled down to nano-scale, there are many new challenges facing the industry. This talk will first discuss the key challenges facing today's technology scaling, including transistor leakage management, process variations and design for manufacturing (DFM). Some innovative technology solutions such as strained Si and 3D transistors will be used to illustrate how to address the technology challenges. The presentation will also discuss how to explore the process-design co-optimization in overcoming these difficulties. Several real technology-product optimization examples, including high-frequency clock tree design and large on-die SRAMs, will be presented on how to mitigate the scaling challenges and achieve optimal product design goals.

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Vivek De

Intel Fellow and Director of Circuit Technology Research in Intel's Circuits Research Lab (CRL)

Vivek De is an Intel Fellow and Director of Circuit Technology Research in Intel's Circuits Research Lab (CRL). He provides strategic direction for future circuit technologies and is responsible for aligning CRL's circuit research with technology scaling challenges.

He has published 151 technical papers in refereed conferences and journals, and 6 book chapters in the areas of low power and high performance circuits. He holds 129 patents, with 64 more patents filed (pending). Vivek received his Bachelor's degree in electrical engineering from the Indian Institute of Technology in Madras, India in 1985 and his Master's degree in electrical engineering from Duke University, Durham, North Carolina in 1986. He received a Ph.D. in electrical engineering from Rensselaer Polytechnic Institute (RPI), Troy, New York in 1992.

Presentation Abstract

Presentation Title	: Energy-Efficient Terascale Computing in Nano
	Technology: Emerging Challenges and Opportu
Presenter Name	: Vivek De
Job Title	: Intel Fellow and Director of Circuit Technolog
	Research in Intel's Circuits Research Lab (CRL)

Abstract:

We will present emerging opportunities to scale new heights in energy-efficiency and cost-effectiveness, and achieve terascale performance levels. We will show how this can be achieved by (1) continued Moore's Law technology evolution into nanoscale regimes; (2) innovative many-core processor architectures containing general-purpose cores, special-purpose engines & efficient on-die interconnect networks; and (3) exploiting the tremendous levels of parallelism in future mainstream applications. We will discuss the challenges and opportunities to enable fast, efficient and fine-grain performance & power management in manycore processors. We will show how designs with multiple independently controlled supply and frequency domains can provide unprecedented levels of energy management capabilities, variation tolerance, reliability and resiliency. We will highlight the barriers & promising solutions to achieving ultra-low-voltage operation and pushing the thermal envelope, both of which are critical for widening the range of dynamic voltage & frequency scaling in future processors.

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Valluri R. Rao

Intel Fellow, Technology and Manufacturing Group Director, Analytical and Microsystems Technologies, Intel Corporation

Valluri Rao pioneered a new infrastructure for VLSI IC characterization which is used for silicon debug and yield improvement of Intel's Microprocessor Products. New technology was developed in R&D labs at Intel and equipment was developed in collaboration with

semiconductor equipment suppliers. This infrastructure was proliferated throughout Intel's worldwide Design, Assembly & Test and Manufacturing Fabs in addition to being adopted by the semiconductor industry at large. Rao was elected to Intel Fellow in the Technology and Manufacturing Group for these accomplishments.

The technology developed included, Electron-Beam Voltage Contrast testing, Magneto-Optic testing for on-chip current measurement from microprocessor power busses, Ultra Fast electro-optic testing for through silicon waveform measurements, Infra Red through silicon emission microscopy, and Focused Ion Beam and laser silicon micromachining methods for on-chip reconfiguring of CMOS circuits. In addition, collaterals such as CAD navigation to locate circuits on a chip, and sample preparation were also developed. Design-For-Test features, to enable optimal use of the capabilities on products, were co-developed with product design and CAD groups and implemented in the chip designs.

Also, roadmaps were created and executed to ensure that the characterization capabilities kept pace with Moore's Law of scaling. Rao was involved in utilizing this infrastructure on 9 generations of Intel Microprocessors through circuit characterization, silicon debug, and yield improvement.

Rao initiated Intel's early work on optical interconnects as a direct extension of the optical measurement work on Silicon. Also, Rao established and built up Intel's MEMS research program in the early 2000s as an extension of the silicon

micromachining for CMOS circuit reconfiguring. This program researched and developed applications of MEMS to Intel's wireless technology for multimode and reconfigurable radios through the fabrication of MEMS RF switches integrated with RF passives in a CMOS process. Currently Rao is researching novel memory materials and MEMS to create high density storage solutions for Intel platforms.

Rao was awarded three Intel Achievement awards (Intel's highest technical award), has 62 issued patents, over 30 publications, and has given numerous invited lectures.

Rao graduated from Cambridge University, UK (Jesus College & Engineering Department) with BA, MA and Ph.D. degrees in Electrical Engineering. He also worked as a post doctoral research fellow at Cambridge prior to joining Intel in 1983. Rao was born in Andhra Pradesh, India.

Presentation Abstract

Presentation Title	: A Review of Emerging Memory Te
Presenter Name	: Valluri R. Rao
Job Title	: Intel Fellow and Director of Circuit
	Research in Intel's Circuits Researc

Abstract:

Current Non Volatile Memory technologies are primarily based on floating gate flash (both NOR and NAND). Looking into the future new memory concepts, materials and device structure are being researched to overcome the challenges of continued scaling of flash memory. Many new candidates have emerged, including Phase Change, Ferro-Electric, Magnetic and MEMS based probe storage memories to name but a few. This talk will describe some of these alternative memory technologies that researchers are pursuing and also the challenges associated with them.

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Raj Yavatkar

Intel Fellow and Director of the Platform Validation Architecture in the Digital Enterprise Group

Dr. Raj Yavatkar is an Intel Fellow and Director of the Platform Validation Architecture in the Digital Enterprise Group. He leads the efforts to introduce design/validation technology innovations to reduce the silicon and platform validation complexity. Dr.

Yavatkar led the formation of the Systems Technology Lab involved in advanced R&D in the areas of system architecture and platform technologies. From 1999 through 2004, he was the Chief Software Architect for Intel's IXP family of network processors.

Dr. Yavatkar received his Ph.D. in Computer Science from Purdue University in 1989 and holds thirteen patents, with more than 25 pending. He is recognized as a leading expert in the networking industry, is an Editor of IEEE Network Magazine, and is the General Chair of ACM/IEEE Sponsored ANCS 2007. Dr. Yavatkar has published more than 30 papers in academic journals and conferences and has co-authored the book, Inside the Internet's Resource Reservation Protocol (RSVP) published by John Wiley.

Presentation Abstract

Presentation Title	: SoC architectures in TerraScale w
	and Opportunities
Presenter Name	: Raj Yavatkar
Job Title	: Intel Fellow and Director of the P
	Validation Architecture in the
	Digital Enterprise Group

Abstract:

With continued transistor scaling and ability to put billion+ transistors on the die, multi-core computing has gone mainstream. That includes an increasingly SoC (System on a Chip) architecture that integrates many different components. By putting 10s of multi-threaded processor cores on a die, the computing industry will soon deliver TeraScale system performance on every desktop. However, such a potential also brings with it an interesting set of challenges in the areas of design/validation, reliability, and computer system architecture, and support for emerging applications. The talk will describe these research challenges as well as potential directions for addressing them.

vorld: Challenges

Platform





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Mary Smiley Director, Emerging Platforms Lab (EPL), Corporate Technology Group

Mary Smiley is the Director of the Emerging Platforms Lab at Intel Corporation. She leads the cross geography lab in pioneering research to conceive, architect, and prototype ultra mobile devices that offer rich understanding of a person and their

environment and to explore health technology for emerging markets.

Throughout her career at Intel, Mary has led the design, development, and implementation of a variety of cutting edge research technologies delivering to a variety of Intel groups and external parties. She drove collaboration with TV Networks (ABC, NBC, Discovery, Scripps, Game Show Network), TV listing provider Tribune Media Services (TMS) and device manufacturers (Evolve Communications) to introduce the concept of interactive television - enabling a user to connect with television programming via Internet interactivity. She delivered Enhanced Television solutions such as NBA Pick n' Play (on demand Internet streaming of NBA events) and The Greeks (educational program w/post show interactive PC content) and a multi-point audio conferencing solution MARS - to 3rd party CenterSpan. She delivered Intercom software (home audio networking) to Intel's Home Networks Operation released to consumers along with Intel AnyPoint[™] Home Network products. Other areas of research included leading programs on platform virtualization, partitioning, reliability and scalable I/O virtualization. Mobile device characterization, provisioning and management.

Presentation Abstract

Presentation Title : Mobility - Redefined Presenter Name : Mary Smiley Job Title : Director, Emerging Platforms Lab (EPL), Corporate Technology Group

Abstract:

Mobile computing in the future - is it just about laptops getting smaller or handhelds getting bigger screens? More of the same - Internet access, productivity applications, mail, calendar? Or is this just the tip of the iceberg? Are there new applications, new usages, new experiences that make mobile computing a more integral fabric of every aspect of our lives? Can machines do more than what they are told to do? Can they bridge the digital and the physical world, be aware of more than just the user's command, anticipate and act on behalf of the user? Can they be more than entertainment or productivity tools? Can they enrich all aspects of lives, going beyond work and play? How do we make this future real? What are the key technical challenges that need to be addressed? What advances are making this future happen? Come listen to Mary Smiley, Director of Intel's Emerging Platforms Lab, talk to the future of the mobile experience from Intel's perspective.





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Herman D'Hooge Innovation Strategist Intel Research

Herman D'Hooge is Innovation Strategist with Intel Research responsible in part for bringing external innovations & innovation practices into Intel.

Previously, he established a user-centered design & innovation competency chartered with

bringing new end-user experiences to personal computing that are informed by real human needs and desires. This human-focused approach involves interdisciplinary teams of ethnographers, user researchers, human factors engineers, industrial designers, interaction designers, technologists and engineers for envisioning and defining future computing platforms and technologies.

Herman joined Intel in 1981 and has held positions in technology research, development, platform architecture, industry evangelism, and management in areas ranging from multi-processor computer architectures, PC system architecture, operating systems, computer security, fault tolerance, distributed systems, computer-telephony integration, "new users, new uses" applications research, and branded consumer products (toys, cameras, audio players).

He received an MS in Electrical Engineering and an MS in Computer Science both from the University of Ghent, Belgium. His professional interests are in understanding how technology can meaningfully impact people's lives and how user-centered methods can be practically applied to inform technology innovation.

Presentation Abstract

Presentation Title: Human-Centered InnovationPresenter Name: Herman D'HoogeJob Title: Innovation StrategistIntel Research

Abstract:

The traditional "build it and they will come" mindset to technology innovation in Intel is gradually being augmented with methods aimed at first trying to understand what humans will find valuable and let that inform technology development. This presentation provides a high-level overview of this humancentered approach to innovation and explores implications for engineering education.





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Vittal Kini Director, Intel India Research Center

Dr. Vittal Kini is Director of the Intel India Research Center (IIRC) at Bangalore. The IIRC is the India presence of Intel's Corporate Technology Group. Dr. Kini leads an organization that researches new platform, systems, and silicon technologies and

develops advanced concept computing platforms around Intel's microprocessors and other silicon products. In his 25-year career with Intel, Dr. Kini has contributed in a wide range of computer systems technology areas. His current and recent work covers platforms ranging from new types of handheld, converged communication devices; to low-power handheld PCs; to interesting evolutions of the familiar notebook PC; and some server and datacenter technologies. A recent key focus of his work has been on system design for high energy efficiency.

Dr. Kini is a B.Tech. (Electronics) alumnus of IIT-Bombay. He received his M.S. and Ph.D. degrees in Electrical Engineering (Computer Engineering) from Carnegie-Mellon University, Pittsburgh, PA. He holds six issued patents and has several others pending. Dr. Kini joined Intel in 1982 and currently resides in Bangalore.

Presentation Abstract

Presentation Title	: Software for multi-core processor
Presenter Name	: Vittal Kini
Job Title	: Director, Intel India Research Cent

Abstract:

Future processors developed by Intel will have more than one core on a die. Multi-core processors will bring tremendous computing power to the desktop PC, enabling new classes of applications. These applications will be written using parallel programming techniques. In this talk we will present the tools Intel has developed to support parallel programming and discuss some of the ideas we are exploring to enable wide-spread adoption of parallel programming.

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Tom Rampone

Vice president of Sales and Marketing Group and General Manager of the Channel Platforms Group

Thomas A. Rampone is vice president of Sales and Marketing Group and general manager of the Channel Platforms Group. As one of Intel channel chiefs, Rampone leads a worldwide channel organization whose charter is to develop innovative products that

meet the unique needs of the emerging markets worldwide and to deliver platform ingredients and solutions to broad channel and local OEM (original equipment manufacturers) customers.

Prior to this position, Rampone was general manager of the User-Centered Platform Solutions Division. He managed the development of Intel's desktop platforms, motherboard products and related industry and technology initiatives. Previously, Rampone was director of the Intel Desktop Boards Operation, where he was responsible for development, delivery and support of Intel's desktop board products. Rampone joined Intel in 1984 as a test development engineer, followed by several engineering and management positions in board design and development.

Rampone, who holds seven patents, received his BSEET from the Oregon Institute of Technology in 1984.

Presentation Abstract

Presentation Title	: CMPC - Integrating Technology for
Presenter Name	: Tom Rampone
Job Title	: Vice president of Sales and Marke
	General Manager of the Channel P

Abstract:

There are about 900,000,000 enrolled students in the world and most are still being taught with 19th century learning models. What's remarkable is how useful these methods still are today as they reflect more than 2000 years of teaching and learning common to most people around the world. Educational systems have been reticent to adopt computing despite its promise – and demonstrable value in many other venues. As a result, very few students make use of computing in their everyday school experience at this time. But this changing: global attention linking education to economic productivity and new technologies have awakened and renewed the possibility of effectively incorporating the benefits of computing into the pedagogical experience. By understanding classrooms as complex systems we can begin to understand the necessary nuance and systemic subtlety associated with incorporating 21st century technologies within the constructs of centuries old teaching methodologies – and do so effectively enhancing the total classroom experience for both teachers and students.

I will talk about the development of the our currently available Intel Powered Classmate PC for schools and specifically call out areas where technological innovation can support the students and teachers in ways appropriate to the classroom, enhancing the value of the educational experience in today's world.

or Local Markets

eting Group and Platforms Group





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Andrew Chien Vice President of Intel Research

Andrew A. Chien is Vice President and Director of Intel Research. Dr. Chien has responsibility for Intel's exploratory research activities including Intel's innovative network of lablets in Berkeley, Pittsburgh, and Seattle. Intel Research is involved in a broad

spectrum of exploratory research including computer circuits, architectures, distributed systems, sensors, robotics, networking, communications, ubiquitous computing, emerging markets and the user experience.

From 1998 to 2005, Chien served as the SAIC Endowed Chair Professor in computer science and engineering, and the founding Director of the Center for Networked Systems (CNS) both at the University of California at San Diego (UCSD). From 1990 to 1998, Chien was a professor in computer science and senior scientist at NCSA at the University of Illinois at Urbana-Champaign. Chien received his B.S. in Electrical Engineering and M.S. and Ph.D. in Computer Science, all from the Massachusetts Institute of Technology.

For more than 20 years, Chien has been a global leader in research and the development of high-performance computing systems. His expertise includes networking, Grids, high performance clusters, distributed systems, computer architecture, high speed routing networks, compilers, and object oriented programming languages. Chien has been recognized as an NSF Young Investigator, ACM Fellow and IEEE Fellow.

Presentation Abstract

Presentation Title	: Exploratory Research: Essential C	
	Computing for the Essence of our	
Presenter Name	: Andrew Chien	
Job Title	: Vice President of Intel Research	

Abstract:

Next generation computing systems will move from task and utility-orientation to supporting the essence of our lives. Intel Research's "Essential Computing" vision is driving a broad-based effort to create applications and systems technologies to simplify and enhance all aspects of our work and daily life. We will describe the Intel Research organization, our vision for essential computing, and highlight our research themes which increase capabilities for computing systems to have personal awareness, be richly communicative, exhibit physicality, conceal complexity, and couple with biological systems. A selection of current research projects and opportunities in these areas will be described.

Computing -Lives

(intel) Education



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TRACK 1: SYSTEM & ARCHITECTURE



Anand Rajan Staff Architect, Digital Enterprise Group Intel Corporation

Presentation Title: Intel® Trusted Execution Technology (TXT)



Krishna Paul Software Architect, Ultra-mobile group

Presentation Title: UMD usage models, technology requirement and research challenges



Arun Chandrasekhar Staff Architect, Digital Enterprise Group

Presentation Title: Systems Packaging: Multi-Disciplinary Challenges

(intel[®]) Education



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TRACK 2: TECHNOLOGY & MANUFACTURING



TS Yeoh Principal Engineer, Assembly Test Manufacturing (ATM), Test Operation

Presentation Title: Systematic innovation in Manufacturing -Challenges/Strategies



G Sreenivas General Manager Technology Manufacturing Group, India (TMG-I) Intel Technology India Pvt. Ltd., Bangalore, India

Presentation Title: Challenges & Oppprtunities in Electronic Packaging



Jeff Pettinato

Senior Principal Engineer, Technology and Manufacturing GroupAutomation Strategy & Pathfinding Manager, Assembly Test Technology Development Intel Corporation

Presentation Title: Highly Productive Assembly and Test Manufacturing in the Nano-Technology Era

TRACK 3: SOFTWARE FOR MULTI-CORE



James Reinders Chief Evangelist and Director of Marketing

(intel[®]) Education

Presentation Title: Exploiting Parallelism with Multi-core Technologies



Young Wang Manager of XML engineering

Presentation Title: Parallelized XML Processing



Milind Girkar Principal Engineer

Presentation Title: Compiler challenges for future computing platforms



Suresh Srinivas Principal Engineer

Presentation Title: Concurrency Control in Managed Runtimes

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TRACK 4: EMERGING TECHNOLOGIES



JM Van Thong Senior staff software engineer, Intel Digital Health Group

Presentation Title: Sensing and making sense: the new challenges of healthcare information systems



Sunit Tyagi Senior Principal Engineer & Director of Technology Intel India

Presentation Title: VLSI Process Technology



Ajay Bakre Research Scientist Intel Research

Presentation Title: Rural Wireless Connectivity: Technologies and Challenges





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TECHNICAL CHAIRS



Sunit Tyagi Senior Principal Engineer & Director of Technology Intel India



G Sreenivas General Manager Technology Manufacturing Group, India (TMG-I) Intel Technology India



Kumar Ranganathan Trusted Platform Research Group



Kalyan Muthukumar Principal Engineer







Ajay Bakre Research Scientist Intel Research



PROFILE OF DELEGATES FROM ACADEMIA



Intel Asia Academic Fo October 24 - 26, 2007, Nev

China

	Name	University	Area of Expertise
1.	Dr. Dian-fu Ma	Beihang University	Grid Computing, Visualization Computing, High Speed Network Computing, High Performance Computing
2.	Mr. Guozhi Xu	Shanghai Jiaotong University	Embedded System
3.	Dr. Hai Jin	Huazhong University of Science and Technology	Computer Architecture, Parallel and Distributed Computing, Grid Computing, High Performance Computing, Peer-to-Peer Computing
4.	Prof. Wan Jinyou	School of Software Engineering, Tongji University	Embedded System
5.	Dr. Jogesh K. Muppala	The Hong Kong University of Science and Technology	Embedded Software, Control-Theoretic Power and Energy Management
6.	Dr. Ming Dong	Shanghai Jiao Tong University	Supply Chain Management, Facility Layout, Operations Research
7.	Mr. Tianzhou CHEN	Zhejiang University, China	Computer Architecture
8.	Dr. Wei LU	Beijing Jiao Tong University	Computer and Information Technique
9.	Mr. Weimin Zheng	Tsinghua University	Parallel computing, Grid computing, Network storage and compiler technology
10.	Mr. Wu Yiping	Huazhong University of Science and Technology	Advanced Electronic Package
11.	Dr. Wu Zhonghai (Jack Wu)	School of Software and Microelectronics, Peking University	Embedded Software and System Engineering, Computer Graphics and Multimedia Technology, Education Information System
12.	Dr. Yufeng Jin	Peking University	Integrated system, advanced packaging for microsystem
13.	Dr. Zhenan TANG	China, DUT	Microelectronic, Fab process, IC design
14.	Dr. Zhiping Yu	Tsinghua University	MOS and nanoelectronic devices: simulation and modeling

India

	Name	University	Area of Expertise
1.	Mrs. P.Chitra	Thiagarajar College of Engineering, Madurai, Tamilnadu	High Performance Comp
2.	Prof. D.K.Subramanian	Indian Institute of Science	Transaction Processing, Software Engineering
3.	Dr. Kolin Paul	IIT, Delhi, India	Works in the area of Ada to understand its use ar embedded systems and biological systems
4.	Mr. S.Rajaram	Assistant Professor, ECE Department, Thiagarajar College of Engineering	VLSI Design
5.	Prof. Ramgopal Rao	IIT, Bombay	Electron Devices & Nand
6.	Prof. Srinivas Bala Mandalika	International Institute of Information Technology, Hyderabad	VLSI and Embedded Sys
7.	Prof. Shankar Balachandran	Indian Institute of Technology, Chennai	Processor Architecture, Scalable CAD Algorithms algorithms
8.	Dr. Aswatha Kumar	Visvesvaraya Technological University (M S Ramaiah Institute of Technology)	Computer Graphics, Com Digital Image Processing Pattern Recognition, Co Artificial Neural Networ
9.	Prof. R.Govindarajulu	International Institute of Information Technology, Hyderabad	Computer Architecture, Programming
10.	Prof. HS Jamadagni	Indian Institute of Science, Bangalore	Computer architecture
11.	Dr. V. Kamakoti	Indian Institute of Technology, Chennai	Test Generation, Function Transactional Memory, F Power estimation
12.	Ms. R. Subashini	National Institute of Technology, Calicut	Systems & Architecture
13.	Ms. Vandana Dixit Kaushik	Harcourt Butler Technological Institute, Kanpur	Maintaining higher stand Research activities
14.	Prof. Vinay Kumar Pathak	Harcourt Butler Technological Institute, Kanpur	Maintaining higher stand Research activities

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, Distributed Databases,	
laptive Computing trying nd implications in I in the modeling of	
oelectronics	
stem Design	
Power Mitigation, s, Cache aware	
nputer Architecture, g, Digital Geometry mputer Vision, ⁻ ks	
Compilers and Parallel	
onal Test Generation, Processor Architecture,	
e, Software for Multicore	
dards in Academic and	
dards in Academic and	
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India

Name	University	Area of Expertise
Dr. Bharadwaj Amrutur	Indian Institute of Science, Bangalore	VLSI Circuits and Systems
Dr. Preeti Ranjan Panda	Indian Institute of Technology, Delhi	Low Power Design, System Level Design
Prof. Sanjeev K Aggarwal	IIT Kanpur	Compilers for High Performance Architectures
Dr. B. Venkataramani	Department of Electronics & Communication Engineering, National Institute Of Technology, Tiruchirapalli	FPGA and SOC based DSP system design, Software defined Radio,UWB
Dr. Ranjani Parthasarathy	College of Engineering, Guindy, Anna University	Computer Architecture
Prof. Madhu Mutyam	International Institute of Information Technology, Hyderabad	Computer Architecture and Low Power VLSI
Prof. Atanu Rakshit	International Institute of Information Technology (I2IT), Pune	Parallel Architecture, Parallel Programming, Parallel Algorithm, Gird Computing
Prof. Manish M Patil	International Institute Of Information Technology Pune	Systems and Architecture
Ms. Suchismita Roy	National Institute of Technology Durgapur, West Bengal	Actively involved in setting up an Intel Multicore PC based Parallel Processing Lab at the Department of Computer Science and Engg. NIT Durgapur. Attended several training programs organized by Intel on Multicore software and programming. Also involved in offering courses on distributed and multicore parallel systems at UG (elective) and PG levels.
Dr. Sandeep Sancheti	National Institute of Technology Karnataka, Surathkal, Mangalore	High Frequency Electronics: Optical, Satellite and Cellular communication Millimetre wave propagation, Optical sensors, Blue-tooth, Active Antennas Microwave integrated circuits, Hetereostructure device modelling
		Information Technology: "Telecom Networks, Data Communication, TCP/IP based communication, Internet technologies, ECADfor design, development and training.
	Name Dr. Bharadwaj Amrutur Dr. Preeti Ranjan Panda Prof. Sanjeev K Aggarwal Dr. B. Venkataramani Dr. Ranjani Parthasarathy Prof. Madhu Mutyam Prof. Madhu Mutyam Nrof. Manish M Patil Ms. Suchismita Roy Dr. Sandeep Sancheti	NameUniversityDr. Bharadwaj AmruturIndian Institute of Science, BangaloreDr. Preeti Ranjan PandaIndian Institute of Technology, DelhiProf. Sanjeev K AggarwalIIT KanpurDr. B. VenkataramaniDepartment of Electronics & Communication Engineering, National Institute Of Technology, TiruchirapalliDr. Ranjani ParthasarathyCollege of Engineering, Guindy, Anna UniversityProf. Madhu MutyamInternational Institute of Information Technology (121T), PuneProf. Atanu RakshitInternational Institute of Information Technology PuneMs. Suchismita RoyNational Institute of Technology Durgapur, West BengalDr. Sandeep SanchetiNational Institute of Technology Karnataka, Surathkal, Mangalore

India

	Name	University	Area of Expertise
25.	Dr. Mukesh A. Zaveri	University: S. V. National Institute of Technology, Surat	Signal Processing (R & I Multi-Core Architecure
26.	Mr. Rakesh P. Gohil	S. V. National Institute of Technology, Surat	Program optimization for architecture
27.	Dr. Dhrubes Biswas	Indian Institute of Technology, Kharagpur	Radio frequency integra technology ventures in Cellular Phone Systems RFICs
28.	Dr. Mainak Chaudhuri	Indian Institute of Technology, Kanpur	Computer Architecture
29.	Prof. Susmita Sur-Kolay	Indian Statistical Institute, Kolkata	Algorithmic CAD-VLSI
30.	Dr. V.K. Ananthashayana	M.S.Ramaiah Institute of Technology Bangalore	DSP, Image Processing, Networking
31.	Dr P.T.Vanathi	PSG College of Technology	VLSI Design, Networkin
32.	Prof. (Dr.) J.P.Raina	Vellore Institute of Technology University (VITU)	Advanced Embedded S -ULSI/UDSM system des Nanoelectronics /Nano SET designs and CNT b PBGC Fiber based system
33.	Ms. Nandini Sidnal	Visvesvaraya Technological University,"Jnana Sangama", Belgaum	Agent Technology and I
34.	Prof. P.V.Ramakrishna	Anna University, Chennai	RF IC (PLL, CDR, MIMOT: Studies (signaling capac based circuit extraction Design
35.	Prof. Huzur Saran	Indian Institute of Technology Delhi, Hauz Khas	Algorithms, Wireless an Networking
36.	Dr. Rajat Moona	IIT Kanpur	Computer Security, Ope Embedded Computing
37.	Dr. Renu Jain	University Institute of Engineering & Technology, CSJM University Kanpur	Artificial Intelligence, Al
38.	Prof. Sanjay Govind Dhande	Indian Institute of Technology Kanpur	Engineering Design & M Engineering, Rapid Prot CAD/CAM, Computer Gr Geometry, Kinematics a Mechanisms

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& D), Optimization for re
n for multi-core
egrated circuits (RFIC) and in Wireless Electronics, ms, communication related
ire
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ng, Machine Intelligence,
king
ed System Designs, design, ano-photonics including IT based Inter-connects ystem design
nd Parallel Processing
OTx/Rx) , Interconnect pacities, coding, ISI, EM ion), Biomedical Implant
and High Speed
Dperating systems, g
, Algorithms
& Manufacturing, Reverse rototyping & Rapid Tooling, Graphics & computational and Dynamics of

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India

	Name	University	Area of Expertise
39.	Dr.(Ms) Sumam David S	National Institute Of Technology Karnataka, Surathkal	VLSI Architectures for Signal Processing
40.	Prof. V Abhai Kumar	PhD (Microwave Engg.,), IIT Madras	RF & Microwaves
41.	Dr. M. Khalid	Vellore Institute of Technology University	
42.	Dr. Shaligram Arvind Digamber	University of Pune	Optoelectronics : Fiber Optic And Optical Waveguide Sensors PC/microcontroller Based Instrumentation Simulation Software Development Biomedical Instrumentation and Sensors

Japan

	Name	University	Area of Expertise
1.	Dr. Kazuaki Murakami	Kyushu University	Many-core processor architecture
2.	Dr. Kenichi Okada	Tokyo Institute of Technology	Analog/RF circuit design

Malaysia

	Name	University	Area of Expertise
1.	Dr. Abu Khari Bin A'ain	Universiti Teknologi Malaysia, Skudai	Design and Test
2.	Dr. Azizan bin Aziz	Universiti Sains Malaysia	Nanomaterials and Lith
3.	Dr. Azman Samsudin	School of Computer Sciences, Universiti Sains Malaysia	Cryptography, Parallel a Computing, and Switch
4.	Dr. Engku Muhammad Nazri bin Engku Abu Bakar	Universiti Utara Malaysia	Multi-criteria Decision I
5.	Dr. Ewe Hong Tat	Multimedia University	Wireless Sensor Netwo
6.	Dr. Jamil Ismail	Universiti Sains Malaysia, Penang, Malaysia	Teaching physical chem scienceResearch and su postgraduates
7.	Dr. Lee Sze Wei	Multimedia University, Malaysia	Wireless Communicatio
8.	Dr. Mohd Nasir Tamin	Universiti Teknologi Malaysia	Fatigue and fracture m solid mechanics

Phillipines

	Name	University	Area of Expertise
1.	Dr. Cedric Angelo. M. Festin	University of the Philippines	Networks and Distribut
2.	Mr. Cesar A. Llorente	De La Salle University	FPGA-based design; Em Reconfigurable computi Building application don
3.	Mr. Conrado D. Monzon	De La Salle University - Dasmariñas	Product Test Engineerir
4.	Dr. Florentino C. Sumera	University of the Philippines	Packaging Polymers
5.	Dr. Henry J. Ramos	University of the Philippines, Diliman, Quezon City	Plasma Science and Tec
6.	Jonee Zunega	Mapua Institute of Technology	Materials Science - Micr
7.	Ms. Maria Theresa A. Gusad	University of the Philippines	RF Integrated Circuit De
8.	Mr. Mark S. Romano	University of the Philippines	Electrodeposition

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nechanics, Computational

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bedded Systems; ing on Intelligent nain
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chnology
oelectronics Packaging
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Taiwan

	Name	University	Area of Expertise
1.	Dr. Chung-Ming Huang	National Cheng Kung University, Taiwan	Multimedia Mobile Network Technologies
2.	Wei Chung Hsu National Chiao Tung University (NCTU) Nen-Fu Huang National Tsing Hua University, Taiwan Chung-Ping Chung National Chiao Tung University, Taiwan		Computer Architecture and Optimizing Compilers
3.			Network Security, High Performance Switch/ Router, P2P video streaming.
4.			Computer Architecture
5.	Polly Huang	National Taiwan University	Sensor Network, Ubiquitous Computing, Multimedia Networking
6.	Sy-Yen Kuo	National Taiwan University of Science and Technology	Dependable Computing and Networks, Sensor Networks and Mobile Computing

Vietnam

	Name	University	Area of Expertise
1.	Nguyen Ba Hoi	University of Da nang - Da nang University of Technology	Digital System
2.	Pham Ngoc Nam	Hanoi University of Technology	Embedded System, Reconfigurable Computing, Computer Architectures
3.	Nguyen Van Duong Ministry of Education and Training		Curriculum Development for Electrical and Electronics Engineering, Information Technology
4.	Nguyen Van Tuan	Da Nang University of Technology	Telecommunication and Digital Systems
5.	Bui Cao Thu	Hochiminh City University of Industry (HUI)	Digital Signal Processing, High Performance Computing
6.	Do Dung Ha	Ministry of Education and Training	Network, OSS, Security and Research
7.	Ho Trung My	Ho Chi Minh City University of Technology	Computer Sciences, Electronics, Telecommunication
8.	Pham Bach Duong	Ho Chi Minh Ho Chi Minh City University of Technical and Education	Robotics, Mechatronics, Electronics
9.	Nguyen Quoc Khoa	Ho Chi Minh City University of Natural Sciences	Automation, Machine Vision, Robotics
10.	Nguyen Vu Thang	Ha Noi University of Technology	VLSI design, Si processing



INTEL ASIA ACADEMIC FORUM 2007 TEAM'S PROFILE





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Brenda Musilli Director of Education, Intel Corporation

Brenda Musilli is the Worldwide Director of Education for Intel Corporation and President of the Intel Foundation. A 25-year Intel veteran, Musilli assumed leadership of Intel Education in 2005, building on her lifelong passion for education.

As Director of Education, Musilli leads the Intel® Education Initiative, a more-than-\$100 million annual, global commitment to accelerate math, science and engineering education, the building blocks of innovation. Intel Education spans more than 50 countries and includes the Intel Science Talent Search (Intel STS), the Intel International Science and Engineering Fair (Intel ISEF), Intel® Teach and the Intel Computer Clubhouse network.

On behalf of Intel Education, Musilli travels extensively worldwide, collaborating with leading educators, government officials and multilateral organizations. A frequent speaker on the issues and challenges surrounding global education, she recently served as guest lecturer at Harvard University's Graduate School of Education and as a member of Intel's delegation to the World Economic Forum meeting in Davos, Switzerland. Musilli is also a member of the World Economic Forum's Global Education Initiative steering board.

Since becoming the Director of Education, Musilli has led Intel's increased commitment, through the Intel Teach program, to training an additional 10 million teachers in the next five years, and recently launched Intel Teach Online to reach a broader segment of the teaching population around the world. Under Musilli's leadership, Intel Education Initiative teacher training has increased significantly, and Intel-sponsored science competitions (Intel STS and Intel ISEF) have set record participation.

Musilli holds a Bachelor of Science degree in economics from University of California, Davis and an MBA degree from University of Santa Clara. She is the 52 proud mother of two school-aged children, Megan and John-Jackson.



Cheng Cheng Loo Regional Program Manager - Asia Intel[®] Education

Cheng Cheng Loo is the manager of Intel's Education initiative in Asia. She is responsible for overseeing the development and management of Intel's education programs across Australia, China, India, Indonesia, South Korea, Japan, Malaysia, Pakistan, Philippines, Sri Lanka, Taiwan, Thailand and Vietnam.

Cheng Cheng joined Intel in 1990 and has held a variety of positions in product planning and marketing prior to her role with Intel Education. She received a B.S. from Campbell University, U.S.A., in Computer Science and Mathematics.





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Jeffrey Cao Intel China Academic Relations Manager

Jeffrey's main responsibility is to design and implement strategic programs related to China academia including universities, research institutions, and governmental technology & education initiatives. The programs cover areas such as Multi-Core architecture, HPC & Grid Computing, Wireless & Mobile Internet, and Technology Entrepreneurship. He also

coordinates external research collaborations for Intel China R&D groups as the lead program manager of Intel China Research Council.

Prior to Intel, He worked at HP where he started as Technical Consultant, worked as Solution Business Consultant, and got promoted to Head of HP China IT School.

Jeffrey earned his bachelor's degree in computer science from Peking University, and MBA from Fordham University.



Jolly Wang is manager of Intel China higher education, her responsibilities include collaboration with key universities, government, industry 3rd parties and stakeholders of Intel internal business divisions, to create and implement long term and short term strategies and programs of Intel China higher Education, to enhance the collaboration between Intel and academia, accelerate academic ecosystem enabling and build good

relationship with universities. She is responsible for bringing the latest Intel technologies into university curriculum, with focused on embedded system, multicore, etc, she also manages the Intel fellowship and pipeline program, organizes campus lectures, academic faculty forum, students contest and other academic events to support Intel reach the goal of accelerating China higher education innovation.

Before Jolly joint Intel in May 2003, she was working at Texas Instruments (TI) for its corporate marketing & communications in China, with focus on public relations, corporate marketing and co-marketing programs management.

Jolly holds a Bachelor of Engineering degree in Management Information System (MIS) of Tianjin University of Commerce. She is member of China International Public Relations Association. Jolly is living in an educational family, her parents are both faculties of Mathematics.

Intel China Higher Education Manager





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Joselito Tulao

Intel Philippines Higher Education Manager

Jay Tulao is the Higher Education Manager for the Intel Cavite Site. He joined Intel Philippines in May 1999 as a Logistics Business Analyst focusing on the Year 2000 program. In 2000, he moved on to lead the Networking and Marketing programs of the Technology Business Group where he focused on marketing the site capabilities and facilitating the

Technology MRC efforts. In 2003, he then took on the role of the site Higher Education Manager to lead the university liaison and efforts on curriculum development, researches and faculty development for the academe.

He graduated with a degree in the Bachelor of Science in Industrial Engineering from the University of the Philippines in 1994 and a Masters in Business Management Degree from the Asian Institute of Management in 1999.



Kai's main responsibility is to design & implement the higher and vocational education programs for the branches of Intel technology and manufacturing group (TMG) in China, including the assembly-test factories in Shanghai, Chengdu and the new 12in Fab in Dalian. Most of his efforts are put in the curriculum enabling, talents pool development, and Intel-

university join research in the manufacturing sciences and technologies.

Kai Qiao

Kai joined Intel China in Feb 2006 as a Quality and Reliability Engineer in the department of assembly-test technology development (ATTD) and started current position from Jun 2007. Before joining Intel, he had been working with Philips for 2 years as an assembly process development engineer in Philips China technology center.

Kai won his bachelor's degree in material science in 2001, and his master's degree in electronic package in 2004 from the same university, Huazhong University of science and technology.

Intel China TMG Higher Education Manager





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Manav Subodh Intel India Higher Education Program Manager

Manav Subodh joined Intel Technology India in 2004. He leads Intel India Higher Education Programs with an objective to foster academia-Intel engagement in technology areas of strategic importance to India site. His main charter is to expand the R&D capabilities in India academia, build skilled pipeline to meet the IT workforce requirements of the industry and develop

the technology ecosystem to support new technology adoption.

Manav's current charter is to drive Multi-Core University Program, technology entrepreneur and incubation programs in engineering institutes of India. He represents Intel in various industry forums and works closely with the government and various industry bodies to help drive a change in the university ecosystem across India. He is an engineer in Electronic and Telecommunications and has done his Masters in Business Administration (MBA).



Mohd Hasri Mohd Harizan Intel Malaysia Higher Education Manager

Mohd Hasri Mohd Harizan is the Higher Education Program Manager for the Intel Malaysia. He joined Intel Malaysia in January 1997 as a Production Superintendent focusing on Chipset Operation and managing a group of Manufacturing Specialist to achieve production output and goal. In 2001, he joined the Government & Public Affairs department and took the role of the site Higher Education Manager to lead the university

liaison and efforts on technical seminar, curriculum development, researches and faculty development for the academe.

He graduated with a degree in the Bachelor of Business Administration from the University of Utara Malaysia in 1995.





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Naoko Yanagiharaz Intel K.K., Education Program Manager - Japan

Graduated with a degree in the Bachelor of Arts in Foreign Studies from Sophia University, Tokyo, Japan.

Joined Toppan Printing Co. Ltd, Tokyo, Japan and worked in Technology Development Division.

Graduated with MBA from Monterey Institute of

International Studies, CA, USA.

Joined ITT World Directories (later VNU World Directories) and worked in a joint venture company with NTT in Tokyo, Japan as product development manager and sales support manager.

Joined Intel K.K., Tokyo Japan in 1999 as Internet Marketing Manager and managed consumer focused company website.

Took Education Program Manager position since 2004.



Trang is the Higher Education Manager for Intel Vietnam from 2007. Trang's main responsibilities include setting directions for the HE program in Vietnam through working with Vietnam universities, Ministry of Education and Training on joint curriculum development and research projects and setting up joint labs, working with internal customers and across

teams with the aim of driving the development and implementation of higher education program strategies mapped to Intel's business goals and growth in Vietnam.

Before joining Intel, Trang had 10 year working experience as project manager for Nouvelle Planete, a Swiss-based NGO, English lecturer for Hanoi University of Business and Management and project assistant for Japan International Cooperation Agency in IT training and capacity building for IT Training Institute, National University Hanoi and Hanoi Agricultural University respectively.

Trang received a bachelor's degree in English language from Hanoi University of Foreign Studies (now named as Hanoi University) in 1998, a bachelor's degree in Foreign Trade from Hanoi Foreign Trade University in 2003 and a master degree in International Relations from International University of Japan in 2005.





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Rachel Liu Intel Taiwan Education Program Manager

Rachel is responsible for all Taiwan local education related programs including Intel ISEF (Intel International Science and Engineering Fair), Higher Education Program, Intel® Teach Program (Intel's teacher training program) and Intel Computer Clubhouse.

Rachel has accumulated solid sales/marketing and project management experiences from her previous jobs at IT companies including business manager at Gartner, responsible for strategic positioning and business development of Gartner research and consulting in Taiwan. Also she works as senior marcom specialist for Adventech, responsible for product marketing and channel incentive program. Before the career in IT industry, Rachel was a journalist and executive producer of Chinese TV System, responsible for the production of "International Watchtower" (an in-depth and knowledge-wise weekly program featuring latest international events).

Rachel obtained her M.A. degree in International Law and Relations from National Cheng-chi University and B.A. degree in Diplomacy also from NCU.



Graduated with a degree in the Bachelor of Science in Applied Physics in 1989 and a PhD degree in Condensed Matter Physics in 1994 from Wesleyan University in United States focusing in wide band-gap semiconductor defects.

Joined Intel Malaysia in May 1995 as a Failure Analysis

Engineer in the Quality and Reliability department and instrumental in enabling successful Intel 0.25, 0.18 and 0.13 um technology Physical Failure Analysis. He then built the Physical Failure Analysis competency for the Malaysia Site Failure Analysis and also enabling Physical Failure Analysis in various other Intel Assembly Test Manufacturing sites.

Siek Kah Hee

In 2000, he then took on the challenge as the Intel Malaysia Site Technical Lab Manager.

In 2004, he embarked on a different position as the Intel Malaysia Education Program manager till today. He is not new to the education programs prior to joining the team as he has been a key contributor in the higher education efforts collaborating with local universities in pipeline and research development.

He has published 8 technical papers while in graduate school and 6 more technical papers while working in Intel.

Intel Malaysia Education Program Manager



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Ashutosh Chadha Education Manager, South Asia

Ashutosh Chadha leads the Intel Education Group for South Asia.

In this direction Ashutosh drives Intel's relationships with various State and Central educational bodies for appropriate ICT integration in education for impacting student learning in order to prepare the learners for

21st centrury requirements. He also works towards supporting initiatives in helping to create models for underserved youth in the community to expose them to technology based learning and higher order thinking. Ashutosh also drives Intel's engagement with the higher education system in the country to forged meaningful partnerships with universities to further the quality of higher education and sustain Intel's technology relationship in India.

Ashutosh has nearly 20 years of experience in the field of education including higher education, K-12 as well as the community segments. Ashutosh is a Science garduate and has done his Management from India majoring in Marketing and Finance.

USEFUL INFORMATION

Delhi is a large city that has emerged through the confluence of many contrasting cultures and traditions. Hence, there is a lot to explore and experience. It can be a confusing place for newcomers, especially since it is always teeming with people from various communities. To make their visit a pleasant one, visitors should follow a few general guidelines.

One should keep a fair amount of the local currency, especially loose change with one while travelling through the city. This way one can avoid having to pay a bit extra at any point.

One should trust one's own judgment when it comes to shopping and should beware of touts and agents. Bargaining is often the norm here (except in the upmarket areas, of course!), so it is a good idea to be aware of the prevailing rates before starting the actual shopping.

If you feel lost or confused approach the traffic policemen to guide you.

Beware of beggars and even mendicants or anybody who approaches you for alms or donations. Keep your wallets safe, as you would anywhere else.

The key is to keep the most valuable things closest to you. You shouldn't remove the security belt when you're out and about, so that's where you'll keep you money, passport, tickets (unless you're about to use them), medical prescriptions, and the like.

For travel health, it is best to use your common sense. Take care what you eat or drink. It is best to carry your own mineral water. Hot tea and coffee are good alternatives.

Contd.



Intel Asia Academic Forum 2007 October 24 - 26, 2007, New Delhi

USEFUL INFORMATION

At a glance:

- Area: 1483 sq. kms
- Altitude: 239 m above sea level
- Density: 9294 persons per sq. Km.
- Languages: Hindi, English, Urdu and Punjabi
- Climate: Extreme Hot in Summer and Cold in Winter
- Maximum Temperature: 46 Degree Celsius
- Minimum Temperature: 04 Degree Celsius
- Expected temperatures end October: Max: low 30C/Min 12C
- Winter: December February
- Spring: March to mid April
- Summer: April end to August
- Autumn: September to November
- Best time to Visit: October to March
- River: Yamuna nTime Zone: GMT/UTC +5.5 nDaylight Saving Start & End: not in use
- Currency: Indian Rupee (Rs)
- Electricity: 230-240V 50HzHz
- Electric Plug Details: South African/ Indian-style plug with two circular metal pins above a large circular grounding pin:
- European plug with two circular metal pins

Emergency Nos.

- Police: 100
- Fire: 101
- Ambulance: 102
- Accident & Trauma: 1099

Given below are some details for all your queries on the AAF 07 to be held in Delhi, India from 24th to 26th Oct 2007.

Q) Where is the conference venue?

FAOs

A) This year the Asia Academic Forum 2007 is being hosted at "The India Habitat Centre" New Delhi, India. For more information on the venue, please refer to the venue page in this book.

Q) Do I have to bear some costs to attend the conference? A) Intel will arrange for the following:

- Airport transfers to & fro
- One single room for 3 nights from 23rd to 25th Oct'07
- Transfers from hotel to conference venue on all days
- Group city tour if you choose

- The cost for the above will be taken care by Intel if you are an invited guest from the academia. For others Intel will make hotel booking with direct payment by guest as billing instructions.

Q) What meals will be taken care by organizers?

A) Breakfast- 23rd to 26th Oct'07 Lunch- 24th to 26th Oct'07

Dinner-24th & 25th Oct'07

Q) How far is the conference venue from the hotel? A) It is a drive of approx 30 to 45 minutes from the hotel to conference venue.

Q) How do I reach the conference venue and return back to the hotel everyday?

A) Shuttle services would be arranged for delegates on all the days of the conference at no cost and delegates would be requested to report at the travel desk for transfers to the venue and the hotel.

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Intel Asia Academic Forum 2007 October 24 - 26, 2007, New Delhi

VENUE DETAILS

Boarding and Lodging Intercontinental Eros Address: Nehru Place, New Delhi, 110019 India Tel: 91-11-41223344

Hotel Regale Inn

Address: A - 2 Chitranjan Park, New Delhi , India Tel: +91 11 2627 0101

Conference Venue

Silver Oak Room- Keynote & Track1 Magnolia- Track2 / Meeting Rooms Habitat World, at India Habitat Centre Address: Lodhi Road, New Delhi - 110003, India

(Entry from Gate number 3 from Vardhaman Marg) Tel: +91 11 2627 0101

Gala Dinner Venue

Royal Ballroom

Intercontinental Eros

Address: Nehru Place, New Delhi, 110019 India Tel: 91-11-41223344

FAOs

Q) How far is the hotel from the airport?

A) The drive would take approx 30 minutes early morning and approx 45 to 60 minutes during peak traffic.

Q) What is the present room tariff at the hotel per person for one night stay? A) The rate is INR 15,500/- including taxes for single room occupancy. If you need extra nights or double room, kindly approach the hotel reception and make a request at your own cost.

The cost for 23, 24 and 25th October will be taken care by Intel for invited guest from the academia. All other extra costs have to be settled by the participants directly.

Q) What all costs are covered?

A) Intel will arrange for the following:

- Airport transfers to & fro
- One single room for 3 nights from 23rd to 25th Oct'07 (for invited guest from academia)
- Transfers from hotel to conference venue on all days
- Breakfast- 23rd to 26th Oct'07
- Lunch- 24th to 26th Oct'07
- Dinner- 24th & 25th Oct'07

Q) What do I have to pay extra?

A) Your mini bar expenses and room service expenses, long distance calls from the room, spa bills, consumption of alcohol or tobacco from the hotel, private taxi ride and extended stay if any.

Q) What is the dress code?

A) Smart Business Casual's is the forum dress code. AAF 2007 badge is mandatory to enter the conference venue and for all outbound activities arranged. National dress for the gala dinner on 25th October 2007.

Cintel





Intel Asia Academic F October 24 - 26, 2007, Nev

CONTACT DETAILS

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