Power Management in the Intel® PXA27x Series Application Processors

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Introduction

The Intel® PXA27x series of processors, including the Intel PXA270 processor, introduces new technologies that advance developers' ability to provide users with optimal performance and longer battery life. The introduction of Wireless Intel SpeedStep® Power Manager technology provides substantial new capabilities in terms of low-power operation. The Intel PXA27x platform also supports Intel® Dynamic Voltage Management, in addition to the dynamic frequency management supported in previous Intel® Personal Internet Client Architecture (Intel® PCA) application processors. Dynamic frequency management enables software developers to write code that dynamically changes the core frequency at which the processor runs, balancing performance with power consumption. The Intel PXA27x platform's use of dynamic frequency management augments that capability by allowing code to change system voltage dynamically, as well as providing support for tying frequency changes to voltage changes.

Wireless Intel SpeedStep Power Manager technology introduces new low-power states. By judicious use of those power states, as well as dynamic frequency management and Intel Dynamic Voltage Management, using the techniques described in this paper software developers can put to good use the power management hardware features and accompanying APIs that are available with the Intel PXA27x application processor, obtaining optimal battery life with their applications.

This article builds on the general power management concepts presented in Building Lean Applications for the Intel® PXA25x Processor Family to include features that are unique to the Intel PXA27x series.

Power State Management under Wireless Intel SpeedStep® Power Manager Technology

The Intel PXA27x series of application processors offers five low-power states, in addition to the fully powered, normal operating state and the non-powered state (where the power source is physically removed from the processor):

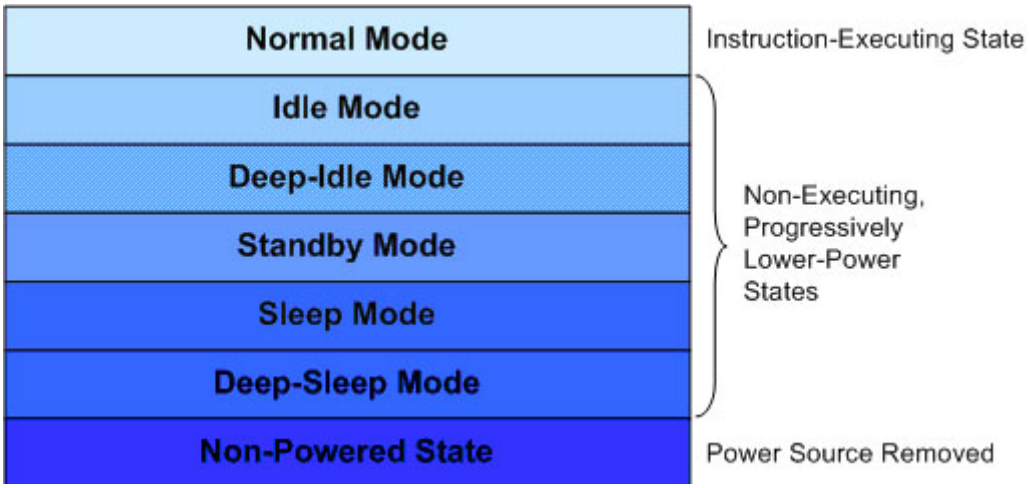

Figure 1. Intel PXA27x series processor power states.

Progressively lower processor power states enable progressively lower requirements on battery resources. Lower power states, however, also carry with them the disadvantages of progressively longer latency periods to return to the instruction executing state, as well as increasingly high degrees of context loss. This context refers to operating information that is required to seamlessly continue a user session or connection to Internet/network resources. It is therefore necessary in application design to write that context information to non-volatile memory (such as flash memory) before entering low power states. These measures not only help to preserve sessions, but they can also be important to preventing system lock-ups upon waking.

Power mode changes are initiated by coprocessor 14, register C7 (PWRMODE); this register also initiates voltage change sequences, including those used in Intel Dynamic Voltage Management, which is discussed below. Writing one of the following values to the PWRMODE[M] bit field initiates the corresponding power mode:

PWRMODE[M] Value	Power Mode
0b000	Normal
0b001 (if the core PLL is enabled)	Idle
0b001 (if the core PLL is disabled	Deep-Idle
0b010	Standby
0b011	Sleep
0b111	Deep-Sleep

Before entering a lowered power state, software must make certain preparations, such as enabling interrupts that will re-wake the system, arrange for retention of system state by setting unit retention bits in the configuration register associated with the lowered power state, and stopping or disabling peripheral devices. Specific preparations vary by power state and the needs of a particular implementation; see the Intel® PXA27x Processor Family Developer's Manual for details. Once a wake event is asserted, the system must reboot if it is in sleep mode or deep sleep mode.

Dynamic Frequency Management in the Intel PXA27x Series

Within normal mode, the Intel PXA270 processor can run at a core frequency that varies from 13MHz to 208MHz, based on the setting of the Core Clock Configuration Register (CCCR) multiplier L. The main clock oscillator is 13MHz, and it drives an on-chip PLL as the clocking source for the processor; that 13MHz speed is generally multiplied by L to set the core run frequency. Normal mode also supports the turbo and half-turbo operating modes, which make it possible for the CPU to run significantly faster than the core frequency.

Dynamic frequency management is enacted by coprocessor 14, register C6 (CLKCFG); when any of the following bits are written to CLKCFG, the system initiates various types of frequency changes, based on settings in the CCCR:

- **CLKCFG[B] – Fast-Bus Mode.** This setting determines whether the system bus runs at the full run mode frequency set in the CCCR (if the CLKCFG[B] bit is set), or at half that frequency (if the CLKCFG[B] bit is clear).
- **CLKCFG[F] – Core Frequency Change.** If the core PLL is enabled in the CCCR and the CLKCFG[F] bit is set, the system stops the core PLL and then restarts it at the frequency reflected in the CCCR settings.
- **CLKCFG[T] – Turbo Mode.** Setting the CLKCFG[T] bit causes the CPU to operate at the Turbo frequency, which is determined by the CCCR[2N] setting. When the CLKCFG[T] bit is set, the CPU operating speed is the core run frequency times *N*. If no changes are made to CLKCFG[B] or CLKCFG[F], the CPU operation speed can be altered by CLKCFG[T] without stopping and restarting the core PLL.
- **CLKCFG[HT] – Half-Turbo Mode.** Whenever CLKCFG[HT] is set (regardless of the state of the CLKCFG[T] bit), the CPU operates at half the turbo frequency. Just as with the CLKCFG[T] bit, changes to the CLKCFG[HT] bit can be enacted without stopping and restarting the core PLL, as long as no changes have been made to CLKCFG[B] or CLKCFG[F].

Dynamic frequency management affords the developer the ability to make changes to the operating frequency without stopping the CPU, which allows applications to make many granular changes to frequency in response to dynamic needs, with minimal impact on performance.

Intel® Dynamic Voltage Management Capabilities

Intel Dynamic Voltage Management is a new capability in the Intel PXA27x processors that augments dynamic frequency management and the power management capabilities of previous generations of processors based on the Intel XScale® technology.

Voltage change sequences in the Intel PXA27x series are initiated by coprocessor 14, register C7 (PWRMODE). The Voltage Manager can initiate either dynamic commands or static commands; dynamic commands are executed while the core is running, whereas static commands are executed while clock to the processor has been disabled. The latter capability supports voltage changes that are coupled with frequency changes that require the PLL to be stopped and restarted.

The following values in the PWRMODE[VC] bit field govern the initiation of voltage changes:

PWRMODE[VC] Value	Voltage Change
0	No voltage change.
1	Initiates a voltage change sequence.

Writes to both PWRMODE[VC] and PWRMODE[M] (see the power state management discussion, above) can be performed in the same operation. Control bits in a series of registers are used to govern voltage change sequences. The following brief listing introduces this mechanism. (For detailed descriptions, see the Intel® PXA27x Processor Family Developer's Manual.)

- **PCFR[FVC] – Frequency/Voltage Change Bit.** Setting this bit in the Power Manager General Configuration Register (PCFR) initiates the voltage change sequencer during a frequency change, if the Power Manager I^2C interface is enabled. This setting can therefore be used to cause a voltage change to be enacted as a result of a frequency change. (The I^2C, or Inter-Integrated Circuit bus, is a specification developed by Phillips; on which the Power Manager interface for the Intel PXA270 processor is based.)
- **PVCR Read Pointer.** This series of bits [24:20] in the Power Manager Voltage Change Control Register (PVCR) points the voltage change sequencer to the Power Manager I^2C Command Register File (PCMDx), a series of 32 registers that can each contain a single voltage change command. The PVCR read pointer controls the execution sequence of PCMD commands by incrementing each time a command is executed, until the last command is reached.
- **PCMD[MBC] – Multi-Byte Command Bit.** Setting this bit enables the use of multi-byte commands by causing the next byte in the PCMDx sequence to be sent without delay or handshaking with the power manager. That mode of execution continues until data is reached with the PCMD[MBC] bit cleared (and the PCMD[LC] bit set, as discussed below).
- **PCMD[DCE] – Delay Command Execution Bit.** Setting this bit causes a pause in command execution equal to a programmable number of 13MHz processor oscillator cycles. That number of cycles is set using the command delay bits in the PVCR and can be any power of 2, up to 2^{24}. This delay capability is useful when, for example, command execution must be paused to allow for stabilization.
- **PCMD[LC] – Last Command Bit.** Setting this bit indicates that the current register within the PCMDx file is the last command to be executed in the command sequence. If this bit is clear, the voltage change sequencer continues execution with the next PCMDx register. Note that if PCMD[LC] is clear in the final register in the PCMDx file (PCMD31), the voltage change sequencer will continue execution with the first register in the sequence (PCMD0).

Intel DFM enables the developer to take more granular control of voltage management than would otherwise be possible by allowing changes to system voltage without stopping the CPU. Like Intel DFM, Intel DVM allows these changes to be made often, in response to the changing needs of the workload, with minimal impact on performance. By supporting interdependency between frequency and voltage changes, the Intel PXA27x series of application processors further increases the flexibility of these mechanisms for the developer.

Conclusion

The advances in the power-management capabilities of the Intel PXA27x series of application processors extend their predecessor technologies significantly. Wireless Intel SpeedStep Power Manager technology provides robust and flexible control that can enable software to prolong battery life in end user devices, leading to an improved user experience. Intel Dynamic Voltage Management and dynamic frequency management allow changes to system voltage and frequency without stopping the CPU, providing additional tools in the developer's arsenal to achieve better balance between performance and prolonged battery life.

Exhaustive information on the topics discussed in this article is available from the Intel® PXA27x Processor Family Developer's Manual. Another resource for developers working to take full advantage of the Intel PXA27x series of processors is a companion article to this one, "Implementing Intel Wireless MMX Technology for the Intel PXA27x Series Application Processors."

About the Author

Matt Gillespie is an independent technical author and editor working out of the Chicago area who specializes in emerging hardware and software technologies. Before going into business for himself, Matt developed training for software developers at Intel Corporation and worked in Internet Technical Services at California Federal Bank. He spent his early years as a writer and editor in the fields of financial publishing and neuroscience. You can reach him at spanningtree@comcast.net.

Additional Resources

- Intel® PXA27x Processor Family Developer's Manual is a comprehensive resource for developers working on applications for the Intel PXA27x series of processors.
- Wireless Intel SpeedStep® Power Manager is the authoritative developer reference for implementation of Wireless Intel SpeedStep technology.
- Intel® PXA27x Family Processor FAQ Page provides a ready reference for key information about high-level concerns of new adopters of the technologies associated with the Intel PXA27x processors.
- Intel® PCA Processors Developer Center helps developers meet the challenges of creating applications for the Intel® Personal Internet Client Architecture (Intel® PCA).
- Mobilized Software Developer Center provides extensive resources to aid in creating software that operates well online and offline, managing transitions between those two states smoothly and managing power optimally.